Terms used: **low power circuits derivatives** Found **41,280** of **213,097**

Sort results by: relevance
Display results: expanded form
Save results to a Binder
Search Tips
Open results in a new window

Try an Advanced Search
Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next
Best 200 shown Relevance scale

1 A fine-grained arithmetic optimization technique for high-performance/low-power data path synthesis
Junhyung Um, Taewhan Kim, C. L. Liu
June 2000 **Proceedings of the 37th conference on Design automation DAC '00**
Publisher: ACM Press
Full text available: pdf(124.57 KB) Additional Information: full citation, abstract, references, citings, index terms

Wallace-tree compressor style has been widely recognized as one of the most effective implementation schemes for arithmetic computation sin VLSI design. However, the scheme has been applied only in a rather restrictive way, that is, for implementing fast multipliers and for generating fixed structures without considering the characteristic of the input signals. The contributions of our work are (1) to extend the applicability of the Wallace scheme to any arithmetic circuit ...

2 Scheduling and resource binding for low power
E. Musoll, J. Cortadella
September 1995 **Proceedings of the 8th international symposium on System synthesis ISSS '95**
Publisher: ACM Press
Full text available: pdf(165.07 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Abstract: Decisions taken at the earliest steps of the design process may have a significant impact on the characteristics of the final implementation. This paper illustrates how power consumption issues can be tackled during the scheduling and resource-binding steps of high-level synthesis. Algorithms for these steps targeting at low-power data-paths and trading off, in some cases, speed and area for low power are presented. The algorithms focus on reducing the activity of the functional units ...

Keywords: adders, data flow graphs, data-path power budget, functional units, high level synthesis, high-level synthesis, logic circuits, low power, low-power data-paths, multipliers, network synthesis, power consumption, resource binding, resource-binding, scheduling, trading off

3 Technology and process aware low power circuit design: An algorithm to minimize leakage through simultaneous input vector control and circuit modification

Nikhil Jayakumar, Sunil P Khatri
April 2007 **Proceedings of the conference on Design, automation and test in Europe DATE '07**
Publisher: EDA Consortium
Full text available: pdf(145.80 KB) Additional Information: full citation, abstract, references

Leakage power currently comprises a large fraction of the total power consumption of an IC. Techniques to minimize leakage have been researched widely. In this paper, we present an approach which minimizes leakage by simultaneously modifying the circuit while deriving the input vector that minimizes leakage. In our approach, we selectively modify a gate so that its output (in sleep mode) is in a state which helps minimize the leakage of other gates in its transitive fanout. Gate replacement i ...

4 In-place delay constrained power optimization using functional symmetries
C. Chang, B. Hu, M. Marek-Sadowska
March 2001 **Proceedings of the conference on Design, automation and test in Europe DATE '01**
Publisher: IEEE Press
Full text available: pdf(146.05 KB) Additional Information: full citation, references, citings, index terms

5 Low power sequential circuit design by using priority encoding and clock gating
Xunwei Wu, Massoud Pedram
August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design ISLPED '00**
Publisher: ACM Press
Full text available: pdf(331.49 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a state assignment technique called priority encoding, which uses multi-code assignment plus clock gating to reduce power dissipation in sequential circuits. The basic idea is to assign multiple codes to states so as to enable more effective clock gating in the sequential circuit. Practical design examples are studied and simulated by PSPICE. Experimental results demonstrate that the priority encoding technique can result in sizable power saving.

6 High-level synthesis techniques for reducing the activity of functional units
E. Musoll, J. Cortadella
April 1995 **Proceedings of the 1995 international symposium on Low power design ISLPED '95**
Publisher: ACM Press
Full text available: pdf(172.83 KB) Additional Information: full citation, references, citings, index terms

7 Energy efficient schedulers in wireless networks: design and optimization
Jeongjoon Lee, Catherine Rosenberg, Edwin K. P. Chong
June 2006 **Mobile Networks and Applications**, Volume 11 Issue 3
Publisher: Kluwer Academic Publishers
Full text available: pdf(392.55 KB) Additional Information: full citation, abstract, references, index terms

Minimizing energy consumption is crucial for portable wireless stations because they operate on a limited battery supply. For example, the IEEE 802.11 standard includes a mechanism called power-saving mode (PSM), which allows a network interface on a mobile station to enter a sleep state whenever possible to reduce its energy consumption. We consider a generic wireless system composed of an access point (AP) and several stations that offer a PSM to its users. Our PSM is AP-centric (i.e., gives c ...

Keywords: energy efficiency, optimization, packet scheduling algorithm, power-saving mode, wireless LAN

8 Static power driven voltage scaling and delay driven buffer sizing in mixed swing QuadRail for sub-1V I/O swings

R. Krishnamurthy, I. Lys, L. Carley

August 1996 **Proceedings of the 1996 international symposium on Low power electronics and design ISLPED '96**

Publisher: IEEE Press

Full text available: pdf(226.83 KB) Additional Information: full citation, references, citings, index terms

9 A physical alpha-power law MOSFET model

Keith A. Bowman, Blanca L. Austin, John C. Eble, Xinghai Tang, James D. Meindl

August 1999 **Proceedings of the 1999 international symposium on Low power electronics and design ISLPED '99**

Publisher: ACM Press

Full text available: pdf(449.78 KB) Additional Information: full citation, references, citings, index terms

10 Session 55: low power circuit design: Elmore model for energy estimation in RC trees

Quming Zhou, Kartik Mohanram

July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**

Publisher: ACM Press

Full text available: pdf(579.69 KB) Additional Information: full citation, abstract, references, index terms

This paper presents analysis methods for energy estimation in RC trees driven by time-varying voltage sources, e.g., buffers, time-varying power supplies, and resonant clock generators. An Elmore energy model that is the computational analog of the conventional Elmore delay model for RC trees is described. Simulation results indicate that the error in energy estimation is less than 2.5% in the worst-case in comparison to HSPICE simulations, with over a 1000X speed-up.

Keywords: Energy estimation, RC trees, interconnect

11 Technologies and devices for low power: Analysis and mitigation of variability in subthreshold design

Bo Zhai, Scott Hanson, David Blaauw, Dennis Sylvester

August 2005 **Proceedings of the 2005 international symposium on Low power electronics and design ISLPED '05**

Publisher: ACM Press

Full text available: pdf(230.47 KB) Additional Information: full citation, abstract, references, citings, index terms

Subthreshold circuit design is a compelling method for ultra-low power applications. However, subthreshold designs show dramatically increased sensitivity to process variations due to the exponential relationship of subthreshold drive current with V th variation. In this paper, we present an analysis of subthreshold energy efficiency considering process variation, and propose methods to mitigate its impact. We show that, unlike superthreshold circuits, random dopant fluctuation is the dominant c ...

Keywords: max of lognormal RVs, subthreshold variability

12 Leakage-aware circuit design: Circuit-aware device design methodology for nanometer technologies: a case study for low power SRAM design

Qikai Chen, Saibal Mukhopadhyay, Aditya Bansal, Kaushik Roy

March 2006 **Proceedings of the conference on Design, automation and test in Europe: Proceedings DATE '06**

Publisher: European Design and Automation Association

Full text available: pdf(369.72 KB) Additional Information: full citation, abstract, references

In this paper, we propose a general *Circuit-aware Device Design* methodology, which can improve the overall circuit design by taking advantages of the individual *circuit characters during the device design phase*. The proposed methodology analytically derives the optimal device in terms of the pre-specified circuit quality factor. We applied the proposed methodology to SRAM design and achieved significant reduction in standby leakage and access time (11% and 7%, respectively, for con ...

13 Power minimization in IC design: principles and applications

Massoud Pedram

January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1

Publisher: ACM Press

Full text available: pdf(550.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design

14 Circuit challenges for scaled technologies: Leakage power reduction by dual-vth designs under probabilistic analysis of vth variation

Michael Liu, Wei-Shen Wang, Michael Orshansky

August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design ISLPED '04**

Publisher: ACM Press

Full text available: pdf(154.37 KB) Additional Information: full citation, abstract, references, citings, index terms

Low-power circuits are especially sensitive to the increasing levels of process variability and uncertainty. In this paper we study the problem of leakage power minimization through dual Vth design techniques in the presence of significant Vth variation. For the first time we consider the optimal selection of Vth under a statistical model of threshold variation. Probabilistic analytical models are introduced to account for the impact of Vth uncertainty on leakage power and timing slack. Using th ...

Keywords: power minimization, variability, yield

15 System design methodologies: Delay optimal low-power circuit clustering for FPGAs with dual supply voltages

Deming Chen, Jason Cong

August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design ISLPED '04**

Publisher: ACM Press

Full text available: pdf(246.72 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a delay optimal FPGA clustering algorithm targeting low power. We assume that the configurable logic blocks of the FPGA can be programmed using either a high supply voltage (high-Vdd) or a low supply voltage (low-Vdd). We carry out the clustering procedure with the guarantee that the delay of the circuit under the general delay model is optimal, and in the meantime, logic blocks on the non-critical paths can be driven by low-Vdd to save power. We explore a set of dual-Vdd com ...

Keywords: circuit clustering, dual supply voltage, low-power FPGA

16 Session 55: low power circuit design: A novel variation-aware low-power keeper architecture for wide fan-in dynamic gates

Hamed F. Dadgour, Rajiv V. Joshi, Kaustav Banerjee

July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**

Publisher: ACM Press

Full text available: pdf(1.90 MB) Additional Information: full citation, abstract, references, index terms

Substantial increase in leakage current and threshold voltage fluctuations are making design of robust wide fan-in dynamic gates a challenging task. Traditionally, a PMOS keeper transistor has been employed to compensate for leakage current of pull down (NMOS) network. However, to maintain acceptable noise margin level in sub-100 nm technologies, large PMOS is necessary, which results in substantial contention (during pull down) and severe loss of performance. In this paper, a novel keeper archi ...

Keywords: VLSI, dynamic gates, keeper design, low-power design, process variation, reliability, robustness

17 Activity-driven clock design for low power circuits

Gustavo E. Téllez, Amir Farrahi, Majid Sarrafzadeh

December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design ICCAD '95**

Publisher: IEEE Computer Society

Full text available: pdf(192.30 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

In this paper we investigate activity-driven clock trees to reduce the dynamic power consumption of synchronous digital CMOS circuits. Sections of an activity-driven clock tree can be turned on/off by gating the clock signals during the active/idle times of the clocked elements. We propose a method of obtaining the switching activity patterns of the clocked circuits during the high level design process. We formulate three novel activity-driven problems. The objective of these problems is to mini ...

Keywords: Power minimization, Sleep Mode, Clock Tree, Gated Clock Tree

18 Issues and directions in low power design tools: an industrial perspective

Jerry Frenkil

August 1997 **Proceedings of the 1997 international symposium on Low power electronics and design ISLPED '97**

Publisher: ACM Press

Full text available: pdf(853.78 KB) Additional Information: full citation, references

19 Technology and process aware low power circuit design: Understanding voltage variations in chip multiprocessors using a distributed power-delivery network

Meeta S. Gupta, Jarod L. Oatley, Russ Joseph, Gu-Yeon Wei, David M. Brooks

April 2007 **Proceedings of the conference on Design, automation and test in Europe DATE '07**

Publisher: EDA Consortium

Full text available: pdf(270.69 KB) Additional Information: full citation, abstract, references

Recent efforts to address microprocessor power dissipation through aggressive supply voltage scaling and power management require that designers be increasingly cognizant of power supply variations. These variations, primarily due to fast changes in supply current, can be attributed to architectural gating events that reduce power dissipation. In order to study this problem, we propose a fine-grain, parameterizable model for power-delivery networks that allows system designers to study locali ...

20 Technology mapping for lower power

Vivek Tiwari, Pranav Ashar, Sharad Malik

July 1993 **Proceedings of the 30th international conference on Design automation DAC '93**

Publisher: ACM Press

Full text available: pdf(767.97 KB) Additional Information: full citation, references, citings, index terms

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Dialog DataStar

options | logoff | feedback | help

databases | easy search

Advanced Search:

Inspec - 1898 to date (INZZ)

limit

Search history:

No.	Database	Search term	Info added since	Results	
CP		[Clipboard]		0	-
1	INZZ	derivative ADJ power	unrestricted	28	show titles
2	INZZ	1 AND circuits	unrestricted	1	show titles

hide | delete all search steps... | delete individual search steps...

Enter your search term(s): Search tips ☐ Thesaurus mapping

whole document

Information added since: or: none
(YYYYMMDD)

search

☐ Images

Select special search terms from the following list(s):

- Publication year 1950-
- Publication year 1898-1949
- Inspec thesaurus - browse headings
- Inspec thesaurus - enter a term
- Classification codes A: Physics, 0-1
- Classification codes A: Physics, 2-3
- Classification codes A: Physics, 4-5
- Classification codes A: Physics, 6
- Classification codes A: Physics, 7
- Classification codes A: Physics, 8
- Classification codes A: Physics, 9

- Classification codes B: Electrical & Electronics, 0-5
- Classification codes B: Electrical & Electronics, 6-9
- Classification codes C: Computer & Control
- Classification codes D: Information Technology
- Classification codes E: Mech., Manufac. & Production Engineering
- Treatment codes
- Inspec sub-file
- Language of publication
- Publication types

Top - News & FAQS - Dialog

Web Results **1** - **1** of **1** for **"microprocessor power simulation"**. (**0.28** seconds)

Tip: Try removing quotes from your search to get more results.

CiNii - 低電力プロセッサアーキテクチャの現状と諸課題- [Translate this page]
Low power Speech DSP Video coding **Microprocessor Power simulation**. 抄録. 本論文は パネル討論の予稿である。主にアーキテクチャレベルでの低消費電力技術について ...
ci.nii.ac.jp/naid/110003316876/ - 32k - Cached - Similar pages

Dialog DataStar

options | logoff | feedback | help

databases | easy search

Advanced Search:

Inspec - 1898 to date (INZZ)

limit

Search history:

No.	Database	Search term	Info added since	Results	
CP		[Clipboard]		0	-
1	INZZ	tullen-d$	unrestricted	0	-
2	INZZ	seng-j	unrestricted	6	show titles
3	INZZ	cai-g$	unrestricted	402	show titles
4	INZZ	3 AND power-sensitive	unrestricted	0	-
5	INZZ	3 AND power	unrestricted	83	show titles
6	INZZ	5 AND microprocessor	unrestricted	6	show titles

hide | delete all search steps... | delete individual search steps...

Enter your search term(s): Search tips ☐ Thesaurus mapping

whole document

Information added since: or: none
(YYYYMMDD)

search

☐ Images

Select special search terms from the following list(s):

- Publication year 1950-
- Publication year 1898-1949
- Inspec thesaurus - browse headings
- Inspec thesaurus - enter a term
- Classification codes A: Physics, 0-1
- Classification codes A: Physics, 2-3
- Classification codes A: Physics, 4-5
- Classification codes A: Physics, 6

- Classification codes A: Physics, 7
- Classification codes A: Physics, 8
- Classification codes A: Physics, 9
- Classification codes B: Electrical & Electronics, 0-5
- Classification codes B: Electrical & Electronics, 6-9
- Classification codes C: Computer & Control
- Classification codes D: Information Technology
- Classification codes E: Mech., Manufac. & Production Engineering
- Treatment codes
- Inspec sub-file
- Language of publication
- Publication types

Top - News & FAQS - Dialog

Web Results **1 - 10** of about **26** for **derivative peak average ratio threshold microprocessor simulation powe**

vlsid General Chair's Message Program Co-Chairs' Message ...
Both measurement and **simulation** results are presented to confirm our design. ..... consume 53% **peak** and 73% **average power** compared to the original circuit. ...
csdl2.computer.org/comp/proceedings/vlsid/1999/0013/00/0013toc.xml - 305k - Cached - Similar pages

[PDF] Low-**Power** Architectural Design Methodologies by Paul Eric Landman ...
File Format: PDF/Adobe Acrobat
simulation is quite fast and provides PRITI with the input **data** streams for the ..... of **peak** and **average power** by as much as 100% and 25%, respectively. ...
bwrc.eecs.berkeley.edu/Publications/1994/theses/lw_pwr_arch_des_meth_Landman/Landman94.pdf - Similar pages

[PDF] Kool Chips Workshop
File Format: PDF/Adobe Acrobat - View as HTML
Ratio data L1 misses. Figure 2: Instruction count reductions and **data** misses decreasing. ..... ing and the design of a low-**power microprocessor** system. ...
systems.cs.colorado.edu/grunwald/Low**Power**Workshop/koolchips-2000-papers.pdf - Similar pages

[PDF] RS/6000 Scientific and Technical Computing: POWER3 Introduction ...
File Format: PDF/Adobe Acrobat
The POWER3 **microprocessor** introduces a new generation of 64-bit ..... the partial **derivatives** and the grid-point **average** of the field variable. The ...
www.redbooks.ibm.com/redbooks/pdfs/sg245155.pdf - Similar pages

[PDF] High-Performance Image Processing Using Special-Purpose CPU ...
File Format: PDF/Adobe Acrobat
prediction mechanism and a central **peak**, since a **threshold** of 128 produces the most ... For integer codes in one **simulation**, the **average** size of instruction ...
www.eecs.berkeley.edu/Pubs/TechRpts/1996/CSD-96-901.pdf - Similar pages

[PDF] Focus: Reservoir Appraisal in the South China Sea
File Format: PDF/Adobe Acrobat
During tests, pressure and temperature. **data** are measured and stored in downhole. recorders that comprise three sections:. gauges, **power** source and memory. ...
www.slb.com/media/services/resources/oilfieldreview/ors92/0492/composite.pdf - Similar pages

[PDF] Sectional Meetings
File Format: PDF/Adobe Acrobat
Peak abundance of clupeids occurred on June 6 with an **average** density of 1037 ..... A custom **microprocessor** system was designed to log the **data** received. ...
https://dspace1.it.ohio-state.edu/dspace/bitstream/1811/22841/1/V082N2_001 - Similar pages

[PDF] chap01.new new
File Format: PDF/Adobe Acrobat
The first way to obtain such **data** is an instruction set **simulator** that inter- ..... the **ratio** of the **average** instruction times to conclude that the machine ...

www.de9.ime.eb.br/.../Computer%20Organization%20And%20Design%20-%20The%20Hardware-Software%20Interface.pdf - Similar pages

[PDF] A Top-Down Approach To IC Design
File Format: PDF/Adobe Acrobat
effective deep sub-micron ASIC design, high-speed **data** path design,. and low **power** design. n. Advanced verification methods addressing high-speed **simulation** ...
www.indovina.us/~mai/a_top_down_approach_to_ic_design.pdf - Similar pages

Webster's Online Dictionary - The Rosetta Edition
APPARATUS & METHOD FOR MEASURING THE **AVERAGE** ASPECT **RATIO** OF NON-SPHERICAL ..... OF DISPERSION COMPENSATED ULTRASHORT OPTICAL PULSES WITH HIGH **PEAK POWER** ...
www.websters-online-dictionary.org/browse/inventions/indexap.html - Similar pages

1 2 3 **Next**

	Type	L #	Hits	DBs	Search Text
33	BRS	L33	35	US-PGPUB; USPAT; USOCR	("4353117" | "4587625" | "4635208" | "4675832" | "4697241" | "4703435" | "4789944" | "4805113" | "4813013" | "4827427" | "4831543" | "4833619" | "4890238" | "4908772" | "4918614" | "4922432" | "4965741" | "4967367" | "4970664" | "5005136" | "5034899" | "5084824" | "5111413" | "5146583" | "5164908" | "5164911" | "5220512" | "5222030" | "5258919" | "5299137" | "5555201" | "T940008" | "T940020").PN.
34	BRS	L34	3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(microprocessor same simula$6) and (power same simula$6) and (cycles same plurality) and (power same (peak or average)) and derivative
35	BRS	L35	2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	"7035785".pn.
36	BRS	L36	1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	"7035785".pn. and derivative

	Type	L #	Hits	DBs	Search Text
25	BRS	L25	1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(cycles same plurality same derivatives) and (microprocessor same power same simulation)
26	BRS	L26	26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(cycles same plurality same derivatives) and (microprocessor same power)
27	BRS	L27	2094	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	((microprocessor or FFT or MOSFET or JFET) same simula$6) and (power same simula$6)
28	BRS	L28	204	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	L27 and derivative
29	BRS	L29	204	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	L27 and derivatives
30	BRS	L30	18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	L27 and (derivatives same cycle)
31	BRS	L31	52	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(microprocessor same simula$6) and (power same simula$6) and (cycles same plurality) and (peak or average)
32	BRS	L32	27	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(microprocessor same simula$6) and (power same simula$6) and (cycles same plurality) and (power same (peak or average))

	Type	L #	Hits	DBs	Search Text
17	BRS	L17	2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	"4896101".pn.
18	BRS	L18	25	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(microprocessor same multicycle)
19	BRS	L19	3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(microprocessor same multicycle) and (simulation simulator simulating)
20	BRS	L20	0	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(microprocessor near multicycle) and (simulation simulator simulating)
21	BRS	L21	1347	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(microprocessor same simula$6) and (power same simula$6)
22	BRS	L22	126	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(microprocessor same simula$6) and (power same simula$6) and (cycles same plurality)
23	BRS	L23	14	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(microprocessor same simula$6) and (power same simula$6) and (cycles same plurality) and derivatives
24	BRS	L24	2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(microprocessor same simula$6) and (power same simula$6) and (cycles same plurality) and derivatives and thresholds and ratio

	Type	L #	Hits	DBs	Search Text
9	BRS	L9	31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	L4 and L6
10	BRS	L10	1196	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(cycle same power same simulation)
11	BRS	L11	55	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(cycle same power same simulation) and (power same derivative)
12	BRS	L12	6606	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(cycle same power same microprocessor)
13	BRS	L13	6606	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(cycle same power same microprocessor) and (microprocessor same power)
14	BRS	L14	512	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(cycle same power same microprocessor) and (microprocessor same power) and derivative
15	BRS	L15	302	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(cycle same power same microprocessor) and (microprocessor same power) and derivative and threshold
16	BRS	L16	210	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(cycle same power same microprocessor) and (microprocessor same power) and derivative and threshold and ratio

	Type	L #	Hits	DBs	Search Text
1	BRS	L1	970	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(low adj power) same circuits same simul$7
2	BRS	L2	25	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	((low adj power) same circuits same simul$7) and (circuits same derivative)
3	BRS	L3	17948	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(circuits same derivative)
4	BRS	L4	1507	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	L3 and (simulation simulator simulating)
5	BRS	L6	31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	L4 and (cycles) and (data same summary)
6	BRS	L5	794	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	L4 and (cycles)
7	BRS	L7	111	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	L4 and (cycles same plurality)
8	BRS	L8	1636	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	L4 andL6